Notice of Allowability	Application No.	Applicant(s)	
	09/695,516	STASZEWSKI ET AL.	
	Examiner	Art Unit	
	Arnold M Kinkead	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Ex. Amdt 11-13-03*.
2. ☒ The allowed claim(s) is/are *1-25*.
3. ☒ The drawings filed on *24 October 2000* are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
8. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No. ____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the margin according to 37 CFR 1.121(d).
9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☐ Notice of References Cited (PTO-892)
2☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No. _____
4☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5☐ Notice of Informal Patent Application (PTO-152)
6☒ Interview Summary (PTO-413), Paper No. 11/13/03
7☒ Examiner's Amendment/Comment
8☒ Examiner's Statement of Reasons for Allowance
9☐ Other .

Arnold M Kinkead
Primary Examiner
Art Unit: 2817

1. An examiner' s amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner' s amendment was given in a telephone interview with Mr. Ronald O. Neerings on Nov. 13, 2003.

The application has been amended as follows:

4. (Currently amended) The digital phase-domain phase-locked loop circuit according to claim 1 further comprising a ~~an all-pass~~ filter operational to pass a phase error generated via the phase detector to generate the phase error.

9. (Currently amended) The digital phase-domain phase-locked loop circuit according to claim 6 further comprising a ~~an all-pass~~ filter operational to pass said phase error generated via the phase detector to generate a filtered phase error.

11. (Currently amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

a direct modulator operational in response to a modulating data signal and a phase error to generate the OTW; and

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the phase error, the phase-locked loop (PLL) including a loop gain multiplier operational to generate a multiplier signal in response to the phase error.

12. (Currently amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock, the digitally-controlled oscillator comprising a voltage controlled oscillator and a digital-to-analog converter operational to generate an oscillator tuning voltage in response to the OTW;

a direct modulator operational in response to a modulating data signal and a ~~filtered~~ phase error to generate the OTW; and

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the ~~filtered~~ phase error, the phase-locked loop (PLL) including a loop gain multiplier operational to generate a multiplier signal in response to the phase error.

13. (Currently amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

a direct modulator operational in response to a modulating data signal and a ~~filtered~~ phase error to generate the OTW, said direct modulator comprising a combinational element feeding the digitally controlled oscillator such that an oscillator gain can be compensated to substantially remove its effects on loop behavior; and

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the ~~filtered~~ phase error, the phase-locked loop (PLL) including a loop gain multiplier operational to generate a multiplier signal in response to the phase error.

14. (Currently amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

a direct modulator operational in response to a modulating data signal and a ~~filtered~~ phase error to generate the OTW;

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the ~~filtered~~ phase error, the phase-locked loop (PLL) including a loop gain multiplier operational to generate a multiplier signal in response to the phase error; and

a direct modulation switch element operational to selectively attenuate a feed-forward path associated with the PLL.

15. (Original) The phase-locked loop system according to claim 14 wherein a path through the direct modulator is defined by a transfer path gain between the modulation switch element and the digitally-controlled oscillator.

17. (Currently amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

a direct modulator operational in response to a modulating data signal and a ~~filtered~~ phase error to generate the OTW; and

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the ~~filtered~~ phase error, said PLL comprising a phase detector feeding a~~n all-pass~~ filter, wherein the phase detector is responsive to the channel selection signal and the modulating data signal to generate said phase error, ~~and wherein the all-pass filter is operational to pass the phase error to generate a filtered phase error,~~ the phase-locked loop (PLL) including a loop gain multiplier operational to generate a multiplier signal in response to the phase error.

18. (Currently amended) A method of operating a digital phase-locked loop (PLL) system comprising the steps of:

(a) providing a phase-locked loop including a digitally-controlled oscillator (DCO) having a gain K_{DCO}, and a phase detector, wherein the DCO is responsive to an oscillator tuning word (OTW) to generate a DCO output clock having a frequency f_V, and further wherein the phase detector is responsive to a channel selection signal, a modulating data signal and the output clock to generate a phase error;

(b) providing a direct modulator operational in response to the phase error and the modulating data signal to generate the OTW;

(c) observing an accumulated phase $\Delta\phi$ in the phase error in response to a given change Δx in the OTW; and

(d) estimating the DCO gain $\hat{K}_{DCO}$, defined by $\hat{K}_{DCO} = \frac{\Delta\phi}{\Delta x} \cdot f_{ref}$ such that a DCO gain can be compensated to substantially remove its effects on loop behavior.

2. The following is an examiner' s statement of reasons for allowance: The examiner could not find fair suggestion in the prior art of record for the PLL circuit as claimed in the independent claims 1,6,11-14 and 17 for the

direct modulation and loop gain multiplier as claimed in addition to the other limitations. For claims 16, 18 and 25, the estimation of the DCO gain; the transfer path gain... and the observation of accumulated phase, were not suggested.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled " Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arnold M Kinkead whose telephone number is 703-305-3486. The examiner can normally be reached on Mon-Fri, 8:30 am -5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner' s supervisor, Robert Pascal can be reached on 703-308-4909. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Arnold M Kinkead
Primary Examiner
Art Unit 2817

Arnold Kinkead
Nov. 14, 2003